LAW OFFICES
McGuireWoods LLP
1750 TYSONS BOULEVARD, SUITE 1800
MCLEAN, VIRGINIA 22102

APPLICATION FOR UNITED STATES LETTERS PATENT

Applicants:	Kangguo CHENG and Dureseti CHIDAMBARRAO
For:	STRAINED SILICON ON A SiGe ON SOI SUBSTRATE
Docket No.:	FIS9-2003-0240

STRAINED SILICON ON A SiGe ON SOI SUBSTRATE

DESCRIPTION

BACKGROUND OF THE INVENTION

Field of the Invention

The invention generally relates to a semiconductor device and method of manufacture and, more particularly, to a semiconductor device that includes strained silicon on a SiGe on a silicon-on-insulator substrate.

Background Description

Various techniques have emerged to improve performance of state of the art semiconductors. One technique involves introducing strain. Strained silicon exhibits improved semiconductor performance due to enhanced transport properties. Biaxial distortion of the crystal lattice in strained silicon improves electron and hole mobility.

Another performance enhancement technique involves providing a semiconductor layer separated from the substrate by an insulating layer. Also known as silicon-on-insulator (SOI), such structures exhibit reduced parasitic capacitance, thereby enabling a semiconductor to function at significantly higher speeds with reduced electrical losses. The result is an appreciable increase in performance and a reduction in power consumption.

By combining strained silicon with SOI the substantial benefits of both technologies may be realized. Unfortunately, however, current methods for forming strained silicon on SOI suffer drawbacks. One such method, the SIMOX method entails implantation of very high doses of oxygen ions at high energy. Upon annealing, the oxygen forms an oxide layer under the surface of the semiconductor. A problem with SIMOX is that it is relatively costly procedure. Another problem is that the high SIMOX annealing temperature (1350°C) limits the concentration of germanium in SiGe-on-insulator substrates. For wafer bonding, which is another method, there are several technical hurdles including optimization of chemical mechanical polish, bonding conditions and the reduction in dislocation density.

The invention is directed to overcoming one or more of the problems as set forth above.

SUMMARY OF THE INVENTION

The invention solves the problems and/or overcomes the drawbacks and disadvantages of the prior art by providing a semiconductor device with an undercut relaxed SiGe layer. Voids beneath the SiGe layer are filled with dielectric. A strained Si layer is formed on the relaxed SiGe layer. The resulting semiconductor structure thus combines the benefits of a defect-free strained Si surface and a silicon-on-insulator substrate.

In a first aspect of the invention, a method of fabricating a semiconductor structure is provided. The method entails forming a $Si_{1-x}Ge_x$ layer on a substrate. A

plurality of channels is then formed in the $Si_{1-x}Ge_x$ layer and the substrate. Next, a portion of the substrate underneath the $Si_{1-x}Ge_x$ layer is removed to form a void in the substrate. The SiGe layer above the void is relaxed. The void and channels are then filled with a dielectric material. A strained Si layer may subsequently be formed on the relaxed SiGe layer.

In a second aspect of the invention, the method includes forming a $Si_{1-x}Ge_x$ layer on a silicon-on-insulator substrate having a first silicon layer, a second SiO_2 layer and a substrate. Next, a first channel and a second channel are formed. Each channel extends through the $Si_{1-x}Ge_x$ layer to the bottom of the first silicon layer of the substrate. The first channel and second channel are substantially parallel. Next, the $Si_{1-x}Ge_x$ layer is undercut to form a void in the first silicon layer of the substrate from the first channel to the second channel. Subsequently, the first and second channels and the void are filled with a dielectric material. Then a strained silicon layer is formed on the $Si_{1-x}Ge_x$ layer.

In a third aspect of the invention, an intermediate semiconductor structure is formed on a substrate. The structure includes a semiconductor substrate and a relaxed $Si_{1-x}Ge_x$ portion on a semiconductor substrate. The relaxed $Si_{1-x}Ge_x$ portion includes one or more channel or trench regions. The structure includes at least one void between the $Si_{1-x}Ge_x$ portion and the substrate. Voids beneath the $Si_{1-x}Ge_x$ layer may be formed by undercutting. The voids may subsequently be filled with dielectric.

In a fourth aspect of the invention, the semiconductor structure includes a first

layer comprised of a strained semiconductor. A second layer comprised of $Si_{1-x}Ge_x$ is provided beneath the first layer. A third layer comprised of a silicon portion and a dielectric portion is provided beneath the second $Si_{1-x}Ge_x$ layer. A fourth layer comprised of an insulator is provided beneath the third layer. A fifth layer comprised of a substrate is provided beneath the fourth layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a silicon-on-insulator wafer for use in accordance with the principles of the invention;

Figure 2 shows a semiconductor structure with a top layer of SiGe in accordance with the principles of the invention;

Figure 3 shows a semiconductor structure with a layer of SiGe capped with a dielectric layer and trenches in accordance with the principles of the invention;

Figure 4 shows a semiconductor structure with a layer of SiGe capped with a dielectric layer and having trenches in accordance with the principles of the invention;

Figure 5 shows a semiconductor structure with a layer of SiGe capped with a dielectric layer, trenches, and an undercut SiGe island in accordance with the principles of the invention;

Figure 6, shows a top view of a cut away section of a structure capped with a dielectric layer, trenches and an undercut SiGe island in accordance with the principles of the invention;

Figure 7 shows a semiconductor structure that is capped with a dielectric layer and has an underlying layer of SiGe, trenches and an undercut area filled with dielectric in accordance with the principles of the invention;

Figure 8 shows a semiconductor structure with a layer of SiGe, trenches and an undercut area filled with dielectric, and dielectric extending vertically above the surface of the SiGe layer into a layer that previously included a dielectric cap;

Figure 9 shows a semiconductor structure with a top layer of strained semiconductor layer formed selectively on SiGe in accordance with the principles of the invention;

Figure 10 shows a semiconductor structure with a top layer of strained silicon formed non-selectively over the entire surface in accordance with the principles of the invention;

Figure 11 shows a field effect transistor formed on a semiconductor structure in accordance with the principles of the invention; and

Figure 12 is a flowchart of a method for producing a strained silicon layer on a SiGe-on-insulator substrate in accordance with the principles of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

The invention enables fabrication of a strained silicon layer on a SiGe-on-insulator substrate. An exemplary methodology in accordance with the invention entails undercutting a SiGe layer to form a relaxed SiGe island, filling the voids with a dielectric and epitaxially growing Si on the relaxed SiGe. The strained Si thus formed can be free of dislocations and misfits. The resulting structure can also be fabricated cost effectively using conventional processing equipment and materials. Additionally, the structure allows a thin SiGe layer, which enables shallow junctions and enhanced device performance.

Referring now to Figure 1, a silicon-on-insulator (SOI) wafer is shown. Such wafers are commercially available starting substrates for various discrete and integrated circuit (IC) semiconductor device applications. The wafer includes a buried silicon oxide (BOX) layer 120 extending across the entire wafer, just below a thin (e.g., 5 to 200 nm) surface layer of device-quality single-crystal silicon 130. The BOX layer 120 provides robust vertical isolation from the substrate 110. The substrate 110 may be silicon, germanium, silicon germanium, aluminum oxide, or any other suitable semiconductor or insulator. Providing an SOI wafer is a first step 1210 of an exemplary process flow as shown in the flowchart of Figure 12.

The SOI wafer may be fabricated using any of various techniques known in the art. By way of example and not limitation, the SOI wafer may be fabricated using the

SIMOX (Separation by IMplanted OXygen) process, which employs high dose ion implantation of oxygen and high temperature annealing to form the BOX layer in a bulk wafer. As another example, the SOI wafer can be fabricated by bonding a device quality silicon wafer to another wafer (the substrate layer) that has an oxide layer on its surface. The pair is then split apart, using a process that leaves a thin (relative to the thickness of the starting wafer), device-quality layer of single crystal silicon on top of the oxide layer (which has now become the BOX) on the substrate layer. The SOI wafer may also be formed using other processes. The method of fabricating the SOI wafer is not critical to this invention.

Next, as shown in Figure 2, a thin device-quality silicon germanium layer (SiGe or $Si_{1-x}Ge_x$) 210 is formed on the device-quality single-crystal silicon layer 130. The $Si_{1-x}Ge_x$ layer 210 may be deposited or grown on the Si layer using conventional techniques such as chemical vapor deposition methods. For example, ultrahigh vacuum chemical vapor deposition (UHVCVD) may be used in a conventional manner to grow a device quality $Si_{1-x}Ge_x$ layer. Other conventional techniques include rapid thermal chemical vapor deposition (RTCVD), low-pressure chemical vapor deposition (LPCVD), limited reaction processing CVD (LRPCVD) and molecular beam epitaxy (MBE). Growth of a $Si_{1-x}Ge_x$ layer is a second step 1220 of an exemplary process flow in accordance with the principles of the invention as shown in Figure 12.

In an exemplary implementation, the thickness of the $Si_{1-x}Ge_x$ layer 210 is below the critical thickness, as is known in the art. The critical thickness, which depends upon

parameters such as growth rate, growth temperature, germanium concentration and the thickness of the underneath silicon layer, is the thickness beyond which defects such as dislocations and misfits form. By way of example, a thickness of approximately 5 to 100 nm would be less than the critical thickness for many fabrications.

Referring to Figure 3, a cap layer 310, may be formed on the $Si_{1-x}Ge_x$ layer 210. The cap layer 310 protects the top surface of the $Si_{1-x}Ge_x$ layer 210 from etching as described more fully below. The cap layer 310 may be comprised of a dielectric material such as silicon nitride (Si_3N_4) or Si_3N_4 atop an oxide (SiO_2) layer. The Si_3N_4 layer may be approximately 20nm to 100nm thick. If the cap 210 includes a SiO_2 layer, the SiO_2 layer may be approximately 3nm to 20nm thick. The SiO_2 and Si_3N_4 layer may be formed by thermal growth on the $Si_{1-x}Ge_x$ layer 210 or by a conventional deposition technique such as low pressure CVD, plasma-assisted CVD, high-density plasma CVD or other suitable processes. For clarity, the cap layer 310 is shown as a single layer in Figure 3. Cap formation is a third step 1230 of an exemplary process flow in accordance with the principles of the invention as shown in Figure 12.

Referring now to Figure 4, channels or trenches 410 and 420 are formed in the cap 310, $Si_{1-x}Ge_x$ 210 and silicon 130 layers, stopping on the BOX layer 120, using conventional dry or wet etching processes. After forming the cap layer 310 atop the $Si_{1-x}Ge_x$ 210, a conventional photoresist mask (not shown), combined with an optional hardmask (not shown), for example, SiO_2, may be formed atop the cap layer 310. The photoresist mask may be patterned utilizing conventional lithography including resist

exposure and development. Trenches 410 and 420 are formed using the patterned photoresist and conventional etching such as dry etching processes, e.g., reactive ion etching (RIE), ion-beam etching, plasma-etching or any combination thereof. Photoresist may be stripped after etching the hardmask, after etching the cap layer or after etching the entire trenches. The remaining SiO_2 hardmask, if any, may be stripped after forming the trenches. The trenches 410 and 420 are dimensioned and spaced to accommodate active regions of the device. Spacing between trenches may, for example, be approximately 100 to 200 nm. Trench or channel formation is a fourth step 1240 of an exemplary process flow in accordance with the principles of the invention as shown in Figure 12.

Referring now to Figure 5, a portion of the SOI beneath the $Si_{1-x}Ge_x$ 210 layer is removed to form a void 520 beneath the $Si_{1-x}Ge_x$ layer 210. The portion 510 of the $Si_{1-x}Ge_x$ layer 210 above the void 520 and between the trenches 410 and 420 becomes relaxed upon removal of the underlying SOI. The SOI may be removed using a conventional selective timed etching process, such as an ammonia, ammonia-based etchant (e.g., tetramethyl ammonium hydroxide (TMAH)), or a mixture of nitric and hydrofluoric acids, for example. The etch time is predetermined by the etch rate and the spacing between the trenches. The etch rate, which depends heavily upon various factors including concentration, temperature and crystallographic orientation, may vary from approximately 0.01 to 1.5 μm/minute. The difference in etch rate between $Si_{1-x}Ge_x$ and pure silicon is attributed to the change in energy band structure by the addition of germanium. The composition of the $Si_{1-x}Ge_x$ layer 210 may be engineered, such that the

bottom surface is considerably more resistant to the etchant than the remaining portion of the $Si_{1-x}Ge_x$ layer 210. For example, the bottom surface may (or may not) have a higher germanium concentration. The cap layer 310 protects the top surface of the $Si_{1-x}Ge_x$ layer 210 from being etched in the process of removing the SOI layer. The timed etch proceeds for sufficient time to remove enough SOI from below the $Si_{1-x}Ge_x$ layer 210 to form a relaxed $Si_{1-x}Ge_x$ portion 510 that is large enough to define or include an active area. The removal of SOI, also referred to as undercutting, is a fifth step 1250 of an exemplary process flow in accordance with the principles of the invention as shown in Figure 12.

Referring now to Figure 6, a top view of a portion of the structure with cap layer 310 over the $Si_{1-x}Ge_x$ layer 210 is shown. Channels 410 and 420 extend parallel or substantially parallel to each other. The dashed border 610 conceptually defines a portion undercut beneath the relaxed $Si_{1-x}Ge_x$ island 510. Un-etched SOI of layer 130 remains outside of the dashed border 610, thus providing structural support beneath the $Si_{1-x}Ge_x$ layer 210. Within the dashed border 610, SOI from layer 130 has been removed by etching as described above. While the dashed border 610 exhibits a square or rectangular shape as shown in Figure 6, those skilled in the art will appreciate that etching may proceed in all directions, possibly at uneven rates depending upon the etchant, etching parameters, crystallographic orientation, and etched material. Thus, the invention is not limited to an etching border of any particular shape.

Optionally, after undercutting, the $Si_{1-x}Ge_x$ layer 210 may be thermally annealed

at a temperature of about 600 to 900°C to ensure that it is relaxed. The anneal can be either a furnace anneal, which may require several minutes, or a rapid thermal anneal (RTA), which may require 1 to 100 seconds.

Next, the trenches and undercut areas are filled with a dielectric, such as SiO_2 710, as shown in Figure 7. The dielectric may be applied in a conventional manner, such as by using an atmospheric CVD process, a low-pressure CVD process or a high-density plasma CVD process, or other suitable methodologies. As SiO_2 exhibits good isotropic properties, even the void 520 beneath the $Si_{1-x}Ge_x$ island 510 may be filled. The surface may then be planarized to remove the excess SiO_2 and leave the vertical channel portions 720 and 730 of the SiO_2 substantially planar with the cap layer 310. The planarization may be achieved by chemically mechanical polishing (CMP) or other suitable planarization methods. The filling of trenches and undercut voids is a sixth step 1260 of an exemplary process flow in accordance with the principles of the invention as shown in Figure 12.

Referring now to Figure 8, the cap layer 310 is removed to expose the relaxed $Si_{1-x}Ge_x$ layer 210. A conventional wet or dry etch may be performed to remove the cap layer, leaving behind the vertical channel portions 720 and 730 of the SiO_2. If the cap layer is comprised of a plurality of layers of different materials, a plurality of wet or dry etch steps may be performed to remove the material. For example, Si_3N_4 in the cap layer may be etched by a mixture of hydrofluoric and ethylene glycol (HF/EG), or hot phosphoric acid (H_3PO_4). SiO_2, if previously formed in the cap layer, may be etched by

buffered hydrofluoric (BHF) or diluted hydrofluoric (DHF). Alternatively, the SiO_2 in the cap layer may be stripped along with Si_3N_4 by a single step of HF/EG etch. Depending upon the etching process, the vertical channel portions 720 and 730 that extend above the $Si_{1-x}Ge_x$ layer 210 may (or may not) be removed. The removal of the cap is a seventh step 1270 of an exemplary process flow in accordance with the principles of the invention as shown in Figure 12.

Referring now to Figure 9, a strained Si layer 910 is formed on the relaxed $Si_{1-x}Ge_x$ layer 210. The strained Si layer may be formed epitaxially on the relaxed $Si_{1-x}Ge_x$ layer 210 using conventional techniques. For example, ultrahigh vacuum chemical vapor deposition (UHVCVD) may be used in a conventional manner to grow a device quality $Si_{1-x}Ge_x$ layer. Other suitable techniques include rapid thermal chemical vapor deposition (RTCVD), low-pressure chemical vapor deposition (LPCVD), limited reaction processing CVD (LRPCVD) and molecular beam epitaxy (MBE). Formation of the strained Si layer is an eighth step 1280 of an exemplary process flow in accordance with the principles of the invention as shown in Figure 12.

If a thick underlying $Si_{1-x}Ge_x$ layer is desired, an epitaxial growth or deposition of additional $Si_{1-x}Ge_x$ may be performed after the cap layer 310 is removed and before formation of the strained Si layer 910. The strained Si layer 910 may then be formed on the thick $Si_{1-x}Ge_x$ layer.

Because Si has a smaller lattice constant (i.e., atom spacing) than Ge, when Si is grown on the $Si_{1-x}Ge_x$ layer 210, the Si is strained in tension. Due to enhanced mobility

of electrons and holes, the strained Si layer provides an attractive platform for fabricating high performance integrated circuits. For example, nFET mobility increases substantially with strain, with the enhancement beginning to saturate at higher strain (e.g., greater than 1.3%). On the other hand, pFET mobility initially exhibits a slight degradation at low amount of tensile strain, but increases linearly with higher strain.

Figure 9 shows an embodiment in which the strained Si layer 910 is grown selectively on $Si_{1-x}Ge_x$ layer 210, not on the vertical channel portion 720 and 730 of the SiO_2, using a process such as molecular beam epitaxy. Figure 10 shows an alternative embodiment in which the strained Si layer 910 is formed in a non-selective manner over the entire surface. In this case, the Si layer 910 also includes the portion 1010 formed above the vertical channel portions 720 and 730 of the SiO_2. After forming the strained Si layer 910, if necessary, the surface may be planarized by chemical mechanical polishing (CMP) or any other suitable processes.

A small amount of carbon may optionally be added during Si growth to form a carbon-doped silicon ($Si_{1-y}C_y$) layer in which the strain is increased further. The value of y in $Si_{1-y}C_y$ may, by way of example, be approximately 0.001 to 0.02. For simplicity, the layer 710 is referred to and shown as a strained Si layer or Si layer hereinafter.

A suitable thickness for the strained Si layer 910 is below the critical thickness, which is the maximum thickness that strained Si can grow on the $Si_{1-x}Ge_x$ layer 210 without forming defects in the crystal structure (e.g., dislocations). By way of example but not limitation, the strained Si layer 910 may be approximately 5 to 100 nm thick. The

epitaxial growth of the Si layer 910 is an eighth step 1280 of an exemplary process flow in accordance with the principles of the invention as shown in Figure 12.

The structures formed, as shown in Figures 4 through 10, are intermediate structures that accommodate formation of semiconductor devices, such as pFETs and nFETs, in accordance with the principles of the invention. One intermediate structure exhibits a void 520 undercut beneath a portion (e.g., island) 510 of the $Si_{1-x}Ge_x$ layer to relax the undercut $Si_{1-x}Ge_x$ portion, as shown in Figure 5. Another intermediate structure, by way of example, exhibits a thin strained semiconductor layer (e.g., a Si layer) 910 epitaxially grown on the $Si_{1-x}Ge_x$ layer 210, as shown in Figure 9. The intermediate structures thus combine the benefits of a thin strained semiconductor layer with the benefits of SOI. Furthermore, the undercutting step obviates the need for costly and potentially problematic process steps, such as SIMOX or wafer bonding, to create the relaxed $Si_{1-x}Ge_x$ layer on SiO_2. Moreover, the formation of a thin strained Si layer 910 on the relaxed $Si_{1-x}Ge_x$ layer 210 is less conducive to defect formation in the strained Si layer 910, than in conventional processes.

Next, standard CMOS processes may be performed to form devices such as field effect transistors on the structure as shown in Figure 11. The device includes source 1110 and drain 1120 regions separated by a strained Si channel 1160 situated on a $Si_{1-x}Ge_x$ layer 1170. A gate oxide 1150 is provided atop the strained Si channel 1160, and a gate conductor 1180 is provided on top of the gate oxide 1150. Spacers 1130 and 1140 are also provided. These components are found in typical field effect transistors and

further explanation is not needed for one of ordinary skill in the art to readily understand the fabrication process of the FET device. Active device formation is a final step 1290 of an exemplary process flow in accordance with the principles of the invention as shown in Figure 12.

Those skilled in the art will appreciate that a process according to the principles of the invention may include steps in addition to those described above and illustrated in the flowchart of Figure 12. Those skilled in the art will also appreciate that a strained Si or $Si_{1-y}C_y$ on $Si_{1-x}Ge_x$ structure formed according to the principles of the invention may be used to support various integrated circuit devices, including devices other than the field effect transistor shown in Figure 11.

Advantageously, the invention provides a semiconductor device with an undercut relaxed SiGe layer. Voids beneath the SiGe layer may be filled with dielectric. A strained Si layer may be deposited on the relaxed SiGe layer. The resulting semiconductor structure combines the benefits of a defect-free strained Si surface and a silicon-on-insulator substrate. The structure may be fabricated cost effectively using conventional processing equipment and materials. Additionally, because the relaxed SiGe layer may be relatively thin, the structure accommodates shallow junctions which reduce junction capacitance.

While the invention has been described in terms of exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with modifications and in the spirit and scope of the appended claims.